

**FEATURES**

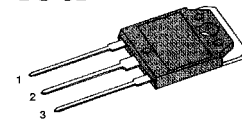
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 25  $\mu$ A (Max.) @  $V_{DS} = 800V$
- Low  $R_{DS(ON)}$  : 1.824  $\Omega$  (Typ.)

$$BV_{DSS} = 800 V$$

$$R_{DS(on)} = 2.2 \Omega$$

$$I_D = 5 A$$

TO-3P



1.Gate 2. Drain 3. Source

**Absolute Maximum Ratings**

Symbol	Characteristic	Value	Units
$V_{DSS}$	Drain-to-Source Voltage	800	V
$I_D$	Continuous Drain Current ( $T_C=25^\circ C$ )	5	A
	Continuous Drain Current ( $T_C=100^\circ C$ )	3.2	
$I_{DM}$	Drain Current-Pulsed	20	A
$V_{GS}$	Gate-to-Source Voltage ①	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy ②	333	mJ
$I_{AR}$	Avalanche Current ①	5	A
$E_{AR}$	Repetitive Avalanche Energy ①	16	mJ
dv/dt	Peak Diode Recovery dv/dt ③	2.0	V/ns
$P_D$	Total Power Dissipation ( $T_C=25^\circ C$ )	160	W
	Linear Derating Factor	1.28	
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	- 55 to +150	$^\circ C$
$T_L$	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

**Thermal Resistance**

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	0.78	$^\circ C/W$
$R_{\theta CS}$	Case-to-Sink	0.24	--	
$R_{\theta JA}$	Junction-to-Ambient	--	40	

**Electrical Characteristics** ( $T_C=25\text{ }^\circ\text{C}$  unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
$BV_{DSS}$	Drain-Source Breakdown Voltage	800	--	--	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	0.97	--	V/ $^\circ\text{C}$	$I_D=250\mu A$ <b>See Fig 7</b>
$V_{GS(th)}$	Gate Threshold Voltage	2.0	--	3.5	V	$V_{DS}=5V, I_D=250\mu A$
$I_{GSS}$	Gate-Source Leakage, Forward	--	--	100	nA	$V_{GS}=30V$
	Gate-Source Leakage, Reverse	--	--	-100		$V_{GS}=-30V$
$I_{DSS}$	Drain-to-Source Leakage Current	--	--	25	$\mu A$	$V_{DS}=700V$
		--	--	250		$V_{DS}=560V, T_C=125\text{ }^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	2.2	$\Omega$	$V_{GS}=10V, I_D=2A$ ④*
$g_{fs}$	Forward Transconductance	--	3.76	--	$\text{S}$	$V_{DS}=50V, I_D=2A$ ④
$C_{iss}$	Input Capacitance	--	1100	1430	pF	$V_{GS}=0V, V_{DS}=25V, f=1\text{MHz}$ <b>See Fig 5</b>
$C_{oss}$	Output Capacitance	--	110	130		
$C_{riss}$	Reverse Transfer Capacitance	--	46	55		
$t_{d(on)}$	Turn-On Delay Time	--	21	50	ns	$V_{DD}=350V, I_D=6A,$ $R_G=11.5\Omega$ <b>See Fig 13</b> ④ ⑤
$t_r$	Rise Time	--	40	90		
$t_{d(off)}$	Turn-Off Delay Time	--	91	190		
$t_f$	Fall Time	--	32	75		
$Q_g$	Total Gate Charge	--	52	68	nC	$V_{DS}=560V, V_{GS}=10V,$ $I_D=6A$ <b>See Fig 6 &amp; Fig 12</b> ④ ⑤
$Q_{gs}$	Gate-Source Charge	--	8.9	--		
$Q_{gd}$	Gate-Drain("Miller") Charge	--	24.7	--		

**Source-Drain Diode Ratings and Characteristics**

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
$I_S$	Continuous Source Current	--	--	5	A	Integral reverse pn-diode in the MOSFET
$I_{SM}$	Pulsed-Source Current ①	--	--	20		
$V_{SD}$	Diode Forward Voltage ④	--	--	1.4	V	$T_J=25\text{ }^\circ\text{C}, I_S=5A, V_{GS}=0V$
$t_{rr}$	Reverse Recovery Time	--	470	--	ns	$T_J=25\text{ }^\circ\text{C}, I_F=5A$
$Q_{rr}$	Reverse Recovery Charge	--	4.96	--	$\mu\text{C}$	$di_F/dt=100A/\mu\text{s}$ ④

**Notes ;**

- ✘ Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- ✘  $L=25\text{mH}, I_{AS}=5A, V_{DD}=50V, R_G=27\Omega$ , Starting  $T_J=25\text{ }^\circ\text{C}$
- ✘  $I_{SD}\leq 5A, di/dt\leq 130A/\mu\text{s}, V_{DD}\leq BV_{DSS}$ , Starting  $T_J=25\text{ }^\circ\text{C}$
- ✘ (Pulse Test : Pulse Width = 250  $\mu\text{s}$ , Duty Cycle  $\leq 2\%$ )
- ✘ ° Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

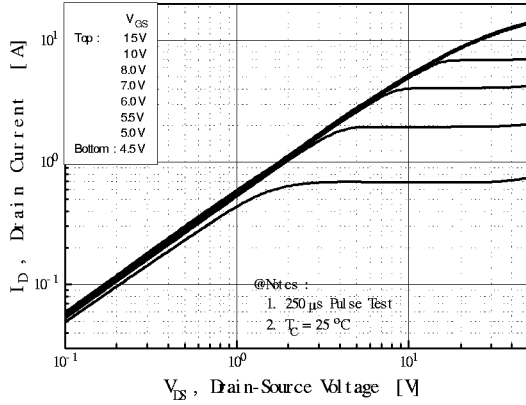


Fig 2. Transfer Characteristics

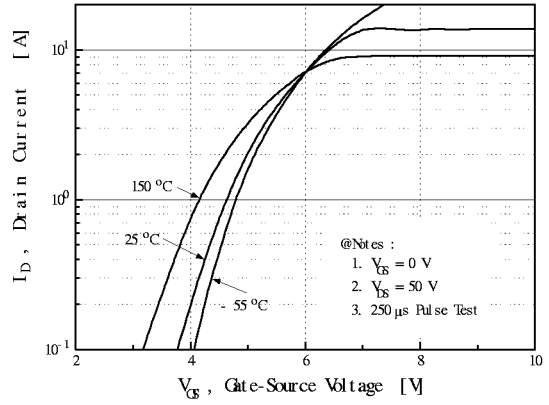


Fig 3. On-Resistance vs. Drain Current

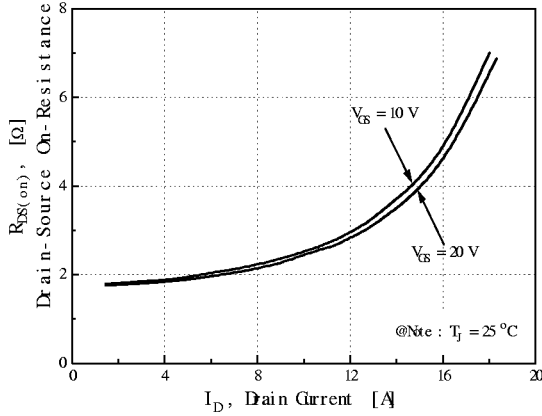


Fig 4. Source-Drain Diode Forward Voltage

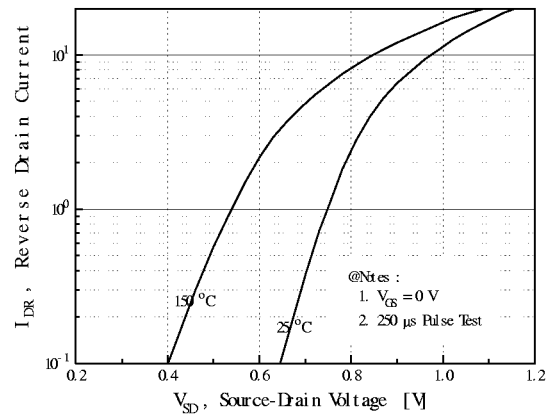


Fig 5. Capacitance vs. Drain-Source Voltage

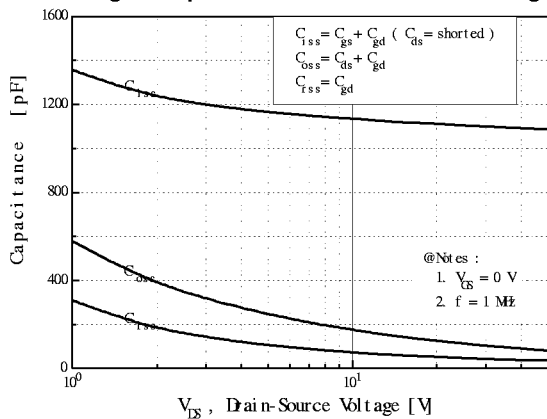
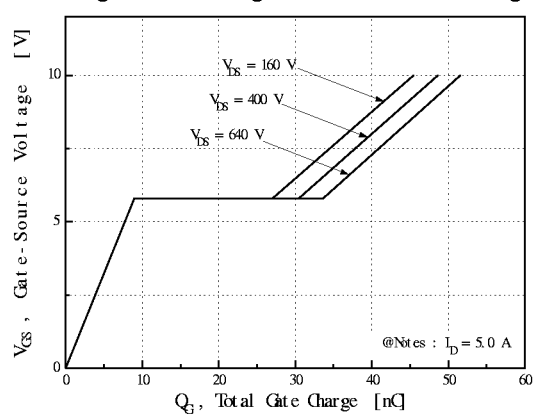


Fig 6. Gate Charge vs. Gate-Source Voltage



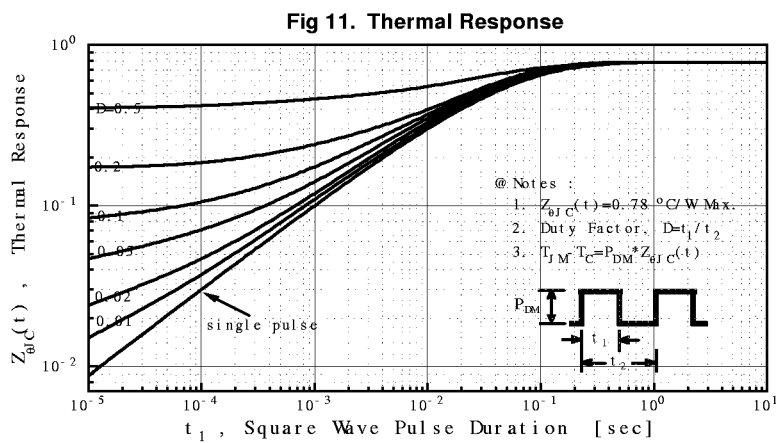
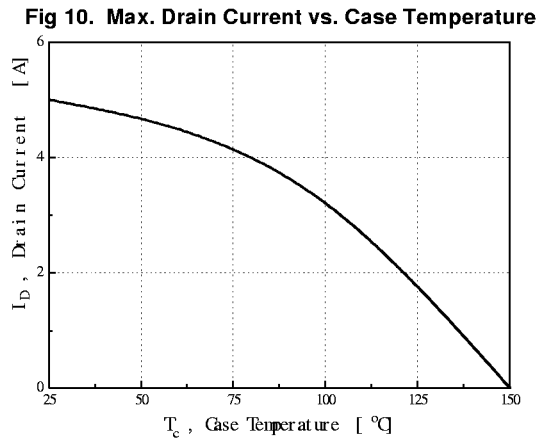
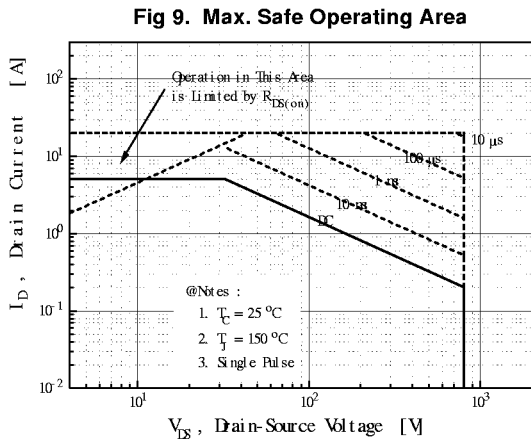
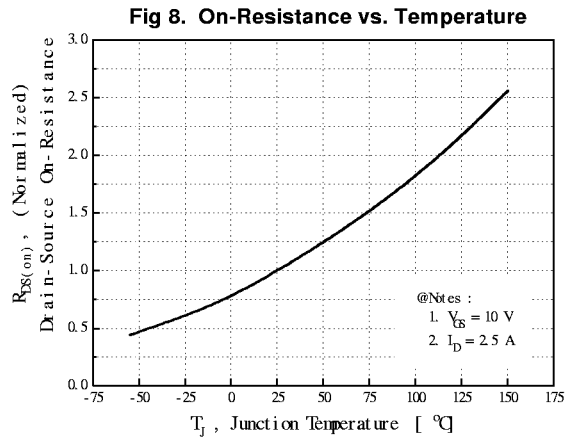
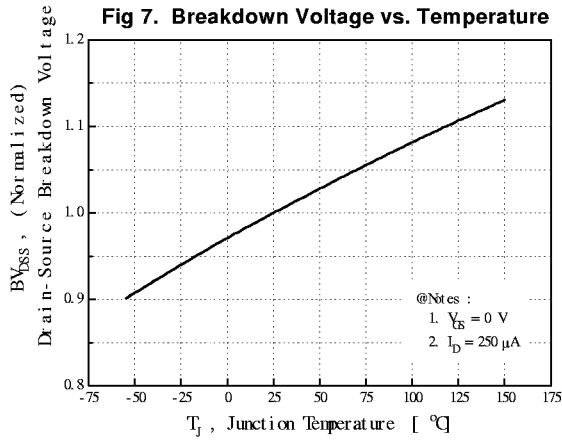


Fig 12. Gate Charge Test Circuit & Waveform

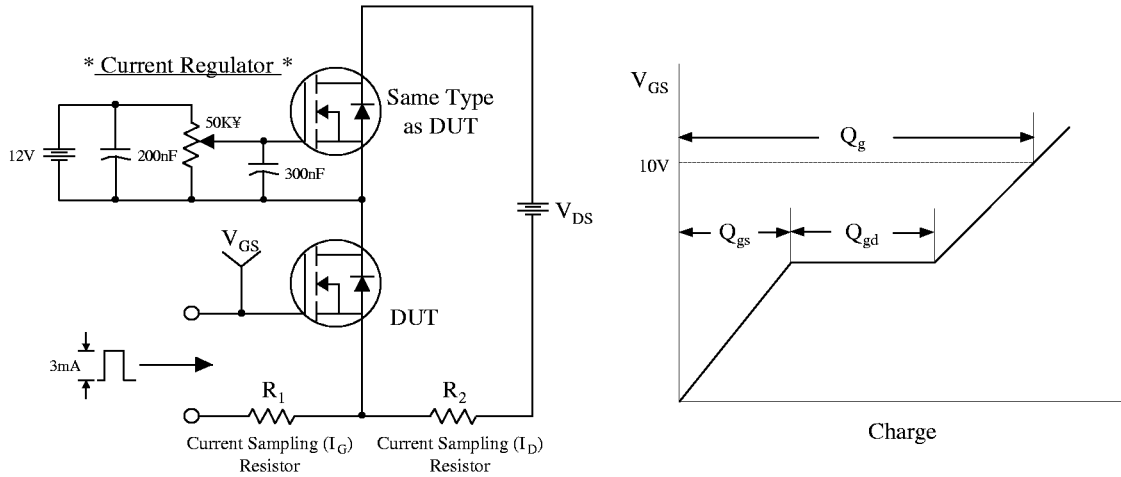


Fig 13. Resistive Switching Test Circuit & Waveforms

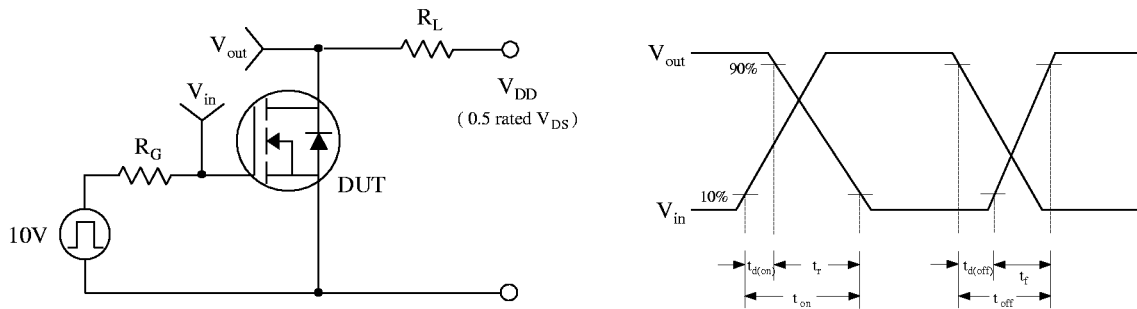


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

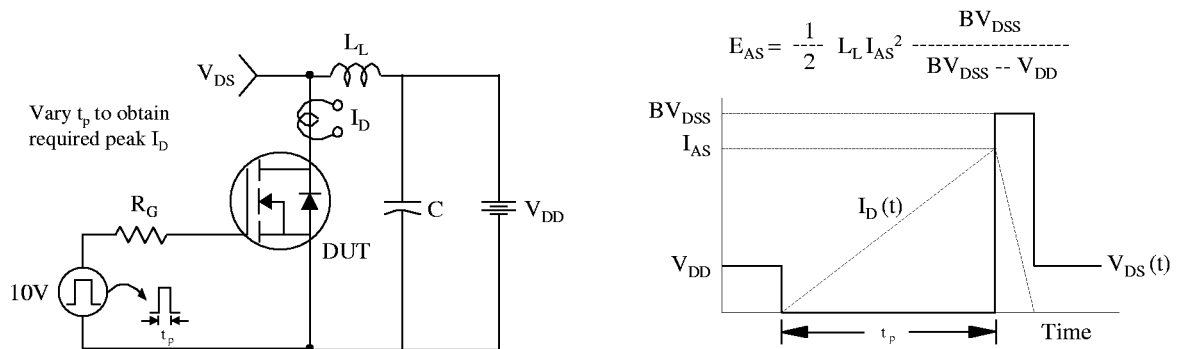


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

